A MINIATURE INTEGRATED MONOLITHIC VCO MODULE

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ABSTRACT

A miniature voltage-controlled oscillator module implementing a novel oscillator/attenuator/buffer amplifier MMIC has been developed for use at 7 GHz. The module provides regulated bias supply for the chip and has been designed for low-cost high-volume automated assembly. Measured performance exceeds goals set forth and matches modeled predictions well.

INTRODUCTION

Voltage-controlled oscillators (VCOs) are widely used in a variety of microwave receiver systems. Typically these components serve as the local oscillator source that drives a mixer used to translate the frequency of an input RF signal over a wide frequency range. With exception of the oscillators described in references [1] and [2], microwave VCOs have traditionally been designed in hybrid form. Monolithic realization of these networks, however, offers several potential advantages. These include component integration at the chip-level, a reduction in circuit size and parts count, greater ease-of-assembly, lower high-volume unit cost, and increased repeatability in unit-to-unit performance.

For these reasons a monolithic chip comprising an oscillator, attenuator, and two-stage buffer amplifier has been designed and incorporated into an integrated VCO module for use in the 7 GHz band. Design goals included a tuning bandwidth greater than 1 GHz for an input tuning voltage of 3-7 V, tuning slope between 150-and 300-MHz/volt, power output greater than 13 dBm, and phase noise less than −70 dBc/Hz at 100 kHz offset. A description of the circuit design, chip fabrication, and module performance follows.

OSCILLATOR DESIGN

The selected oscillator topology is shown in Figure 1. Through capacitive termination of the device source, wideband instability is attained. Termination of the gate terminal with a series high-impedance

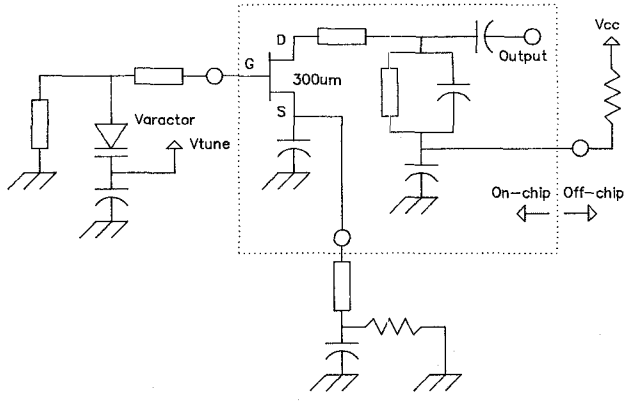

Figure 1. Equivalent Circuit for VCO Network.

transmission line and shunt varactor yields a network capable of meeting tuning bandwidth and slope requirements that were set forth. By varying the varactor capacitance through adjustment of an applied DC voltage, the resonant frequency of the oscillator network is set. Tuning linearity is achieved largely by matching the capacitance slope of the varactor to the reactance slope of the remaining network.

A standard 300 μm gate-width low-noise MESFET is used as the active device in the oscillator. Its choice best compromises tradeoffs between high gain, maximum output power, minimum phase noise contribution, and correlation between modeled and measured performance. By using an internally developed harmonic balance nonlinear analysis program, (ref. [3], [4]), constant power contours for the chosen device were derived for various drain loads and plotted on a Smith chart. From this data a simple drain network was synthesized for optimum output power over the design bandwidth.

Stability analysis was performed by separating the resonant gate network from the active device in a manner described by Basawapatna, et al. (ref. [5]). Figure 2 presents a simplified oscillator used in this analysis. Oscillation occurs when the following small-signal conditions are met:

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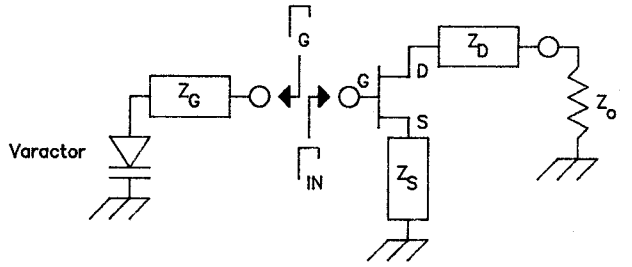

Figure 2. Simplified Oscillator Network Used for Stability Analysis.

$$|\Gamma_G| * |\Gamma_{IN}| \geqq 1 \qquad (1)$$

$$\angle \Gamma_G + \angle \Gamma_{IN} = 0 \qquad (2)$$

where $\Gamma_G$and Γ_{IN} are the respective gate and active network reflection coefficients. During steady state operation the product of $|\Gamma_G|$ and $|\Gamma_S|$ will equal 1. By multiplying the Γ_G and Γ_{IN} phasors together and simultaneously plotting the resulting magnitude and phase, a simple graphical method for determining stability was implemented. Figure 3 shows an example plot in which three values of varactor capacitance were used to simulate tuning. The frequency of oscillation for each case is predicted to be the point where the phase crosses 0° and magnitude is greater than 1.0. Circuit elements were optimized to give a phasor product magnitude greater than 1.2, thus allowing a margin for modeling error and device variation.

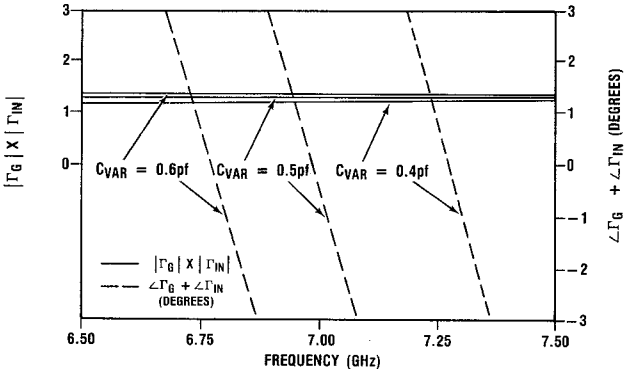

Figure 3. Graphical Method of Calculating Oscillator Instability for Varying Varactor Capacitance (C_{VAR}).

The gate and source networks of the oscillator were selected and then optimized for linear tuning of the resonant frequency versus applied varactor voltage. Quarter-wave shorted stubs for the gate and source bias return networks were realized off-chip to minimize die size and reduce coupling interaction between adjacent structures.

Due to a nonlinearity in monolithic varactor capacitance versus applied DC voltage, it was necessary to utilize an off-chip GaAs hyper-abrupt varactor diode to maintain the tuning slope between 150- and 300-MHz/volt for a 3- to 7 volt tuning voltage range. The varactor model used in circuit analysis was derived from capacitive and s-parameter measurements of several devices.

AMPLIFIER DESIGN

The inherent low quality factor of a varactor-tuned oscillator renders its performance sensitive to load variations. For this reason it was necessary to buffer the oscillator output with an attenuator and two stages of amplification on chip. Figure 4 presents a diagram of these elements. The attenuator is a standard tee-network using GaAs mesa resistors. Each amplifier stage uses a simple shunt inductive/capacitive/resistive feedback to flatten gain over a wide frequency range and minimize temperature sensitivity. Rectangular inductors are used as bias and tuning elements to minimize chip size. Self-bias for all three devices eliminates the need for a negative voltage power supply in the module.

A photograph of the resulting chip, which combines the oscillator, attenuator, and amplifier functions, is shown in Figure 5. The die size measures 1.2 x 2.5 x 0.1 mm.

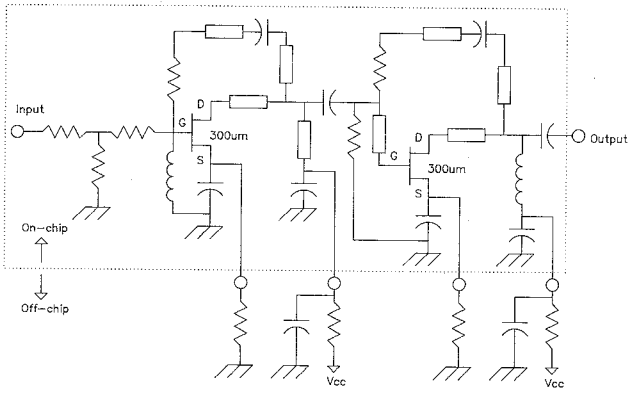

Figure 4. Equivalent Circuit for Attenuator and Two-Stage Amplifier Network.

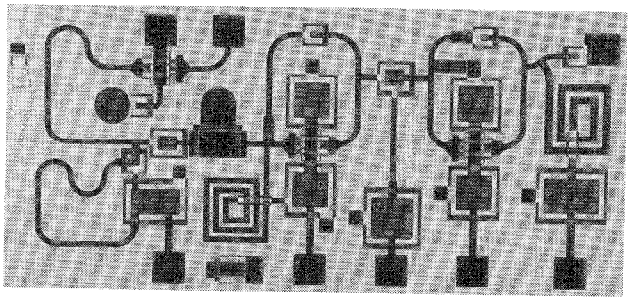

Figure 5. Photograph of Monolithic VCO Chip.

MODULE DESIGN

A thin film network was designed to incorporate the off-chip tuning and bias networks previously described. Size and spacing of bonding pads for both the chip and the thin film network were designed for compatibility with automated assembly. A +5 volt regulator network for the chip was designed that incorporates a standard silicon regulator chip and associated filter capacitors.

These elements were integrated together with the varactor diode and various chip capacitors into a housing measuring 7.6 x 9.9 x 2.5 mm (outside dimensions). Packaging the VCO network with its own regulator in this fashion significantly reduces oscillator phase noise and frequency pulling caused by interaction with other system components. A photograph of the module is shown in Figure 6.

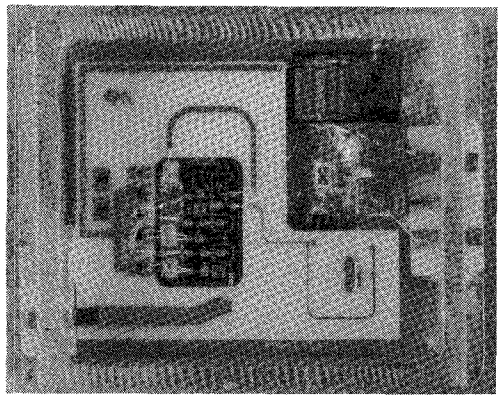

Figure 6. Photograph of Integrated Monolithic VCO Module.

CIRCUIT FABRICATION

Monolithic circuits were fabricated in TI's DSEG GaAs facility. Dual-recess MESFET devices were formulated on ion-implanted wafers optimized for low-noise and high-gain operation. FET gate lengths are 0.5 μm and were defined using electron-beam lithography. MIM capacitors were constructed using 2000 Angstrom thick silicon nitride. The substrate thickness was ground to 0.1 mm, and backside vias were formed by reactive ion etch (RIE).

MODULE PERFORMANCE

The resulting module performance exceeds the requirements set forth for this design. Five units have been tested to date and have demonstrated consistent performance. Figure 7 shows a comparison of predicted and typical measured resonant frequency versus applied tuning voltage. A maximum 35 MHz error between measured and predicted is found for a tuning voltage of 7 volts. Flexibility in setting the center frequency can be achieved through interchange of varactors with differing capacitance and in

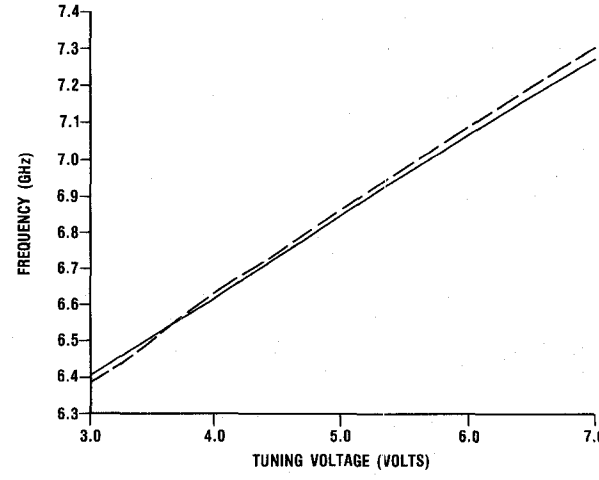

Figure 7. Frequency Response of VCO Module Versus Applied Tuning Voltage.

adjustment of the varactor bond wire length. Figure 8 shows a good match between predicted and typical measured tuning slope which averages 230 MHz/volt (measured) without a linearizing network. Nonlinearities in this response are attributed largely to measurement uncertainty in the applied tuning voltage and resonant frequency. This data shows a slope variation of less than 1.6 to 1 over the measured bandwidth. Bandwidth can be extended an additional 1 GHz by increasing varactor tuning voltage to 15 volts. However, the accompanying tuning slope decreases to 100 MHz/volt in this region. No discontinuities have been discovered in the entire tuning range, and no spurious oscillations have been detected through 22 GHz.

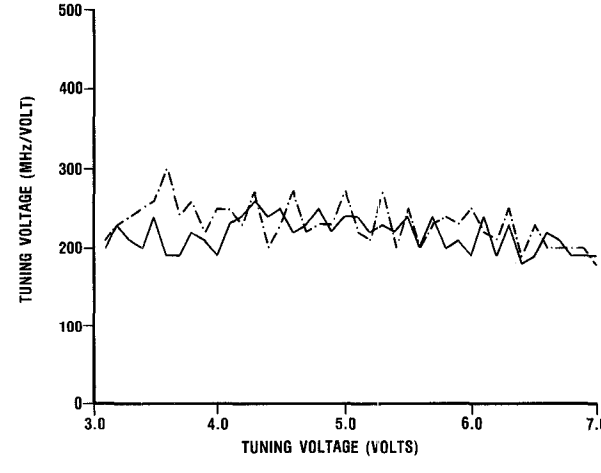

Figure 8. Tuning Slope of VCO Module Versus Applied Tuning Voltage.

Other parameters measured at room temperature include 15 ± 0.2 dBm power output across a 1 GHz band, less than – 80 dBc/Hz phase noise at 100 kHz offset, greater than 22 dBc rejection of the second harmonic, and ± 7.5 MHz frequency pulling with a 3:1 VSWR load at any phase. Drain voltage for the chip is regulated at 5 volts, and total current consumption is 100 mA.

CONCLUSION

A miniature monolithic VCO module has been successfully developed for future high volume manufacture that exceeds performance goals and matches modeling predictions well.

ACKNOWLEDGEMENTS

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